PCT WORLD INTELLECTU[AL] PROPERTY ORGANIZATION
Inte[rnational] Bureau

INTERNATIONAL APPLICATION PUBLISHED UNDER THE PATENT COOPERATION TREATY (PCT)

(51) International Patent Classification 6 : H03K 3/356 — A1

(11) International Publication Number: WO 96/10866

(43) International Publication Date: 11 April 1996 (11.04.96)

(21) International Application Number: PCT/US95/12094

(22) International Filing Date: 18 September 1995 (18.09.95)

(30) Priority Data:
08/315,913 30 September 1994 (30.09.94) US

(71) Applicant: RAMBUS, INC. [US/US]; 2465 Latham Street, Mountain View, CA 94040 (US).

(72) Inventor: JOHNSON, Mark, G.; 125 Arbuelo Way, Los Altos, CA 94022 (US).

(74) Agents: VINCENT, Lester, J. et al.; Blakely, Sokoloff, Taylor & Zafman, 7th floor, 12400 Wilshire Boulevard, Los Angeles, CA 90025-1026 (US).

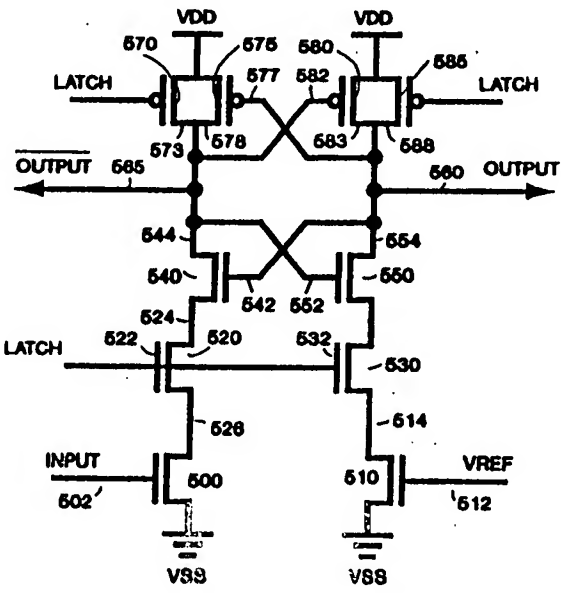
(81) Designated States: AM, AT, AT (Utility model), AU, BB, BG, BR, BY, CA, CH, CN, CZ, CZ (Utility model), DE, DE (Utility model), DK, DK (Utility model), EE, EE (Utility model), ES, FI, FI (Utility model), GB, GE, HU, IS, JP, KE, KG, KP, KR, KZ, LK, LR, LT, LU, LV, MD, MG, MK, MN, MW, MX, NO, NZ, PL, PT, RO, RU, SD, SE, SG, SI, SK, SK (Utility model), TJ, TM, TT, UA, UG, UZ, VN, European patent (AT, BE, CH, DE, DK, ES, FR, GB, GR, IE, IT, LU, MC, NL, PT, SE), OAPI patent (BF, BJ, CF, CG, CI, CM, GA, GN, ML, MR, NE, SN, TD, TG), ARIPO patent (KE, MW, SD, SZ, UG).

Published
With international search report.
Before the expiration of the time limit for amending the claims and to be republished in the event of the receipt of amendments.

(54) Title: CMOS DYNAMIC LATCHING INPUT BUFFER CIRCUIT

(57) Abstract

A CMOS dynamic latching input buffer circuit is described. The input buffer circuit is used to interface integrated circuits with external circuitry. The input buffer circuitry uses a single latch signal. The input buffer minimizes excess capacitance on critical nodes (560, 565) and charge and capacitive "kick-back" into the latching circuit inputs (502, 512). In addition, the input buffer circuit dissipates substantially zero d.c. power.



FOR THE PURPOSES OF INFORMATION ONLY

Codes used to identify States party to the PCT on the front pages of pamphlets publishing international applications under the PCT.

AT	Austria	**GB**	United Kingdom	**MR**	Mauritania
AU	Australia	**GE**	Georgia	**MW**	Malawi
BB	Barbados	**GN**	Guinea	**NE**	Niger
BE	Belgium	**GR**	Greece	**NL**	Netherlands
BF	Burkina Faso	**HU**	Hungary	**NO**	Norway
BG	Bulgaria	**IE**	Ireland	**NZ**	New Zealand
BJ	Benin	**IT**	Italy	**PL**	Poland
BR	Brazil	**JP**	Japan	**PT**	Portugal
BY	Belarus	**KE**	Kenya	**RO**	Romania
CA	Canada	**KG**	Kyrgyzstan	**RU**	Russian Federation
CF	Central African Republic	**KP**	Democratic People's Republic of Korea	**SD**	Sudan
CG	Congo			**SE**	Sweden
CH	Switzerland	**KR**	Republic of Korea	**SI**	Slovenia
CI	Côte d'Ivoire	**KZ**	Kazakhstan	**SK**	Slovakia
CM	Cameroon	**LI**	Liechtenstein	**SN**	Senegal
CN	China	**LK**	Sri Lanka	**TD**	Chad
CS	Czechoslovakia	**LU**	Luxembourg	**TG**	Togo
CZ	Czech Republic	**LV**	Latvia	**TJ**	Tajikistan
DE	Germany	**MC**	Monaco	**TT**	Trinidad and Tobago
DK	Denmark	**MD**	Republic of Moldova	**UA**	Ukraine
ES	Spain	**MG**	Madagascar	**US**	United States of America
FI	Finland	**ML**	Mali	**UZ**	Uzbekistan
FR	France	**MN**	Mongolia	**VN**	Viet Nam
GA	Gabon				

CMOS DYNAMIC LATCHING INPUT BUFFER CIRCUIT

FIELD OF THE INVENTION

This invention pertains to the field of input buffer circuitry for interfacing integrated circuits with external circuitry. More particularly, this invention relates to improving the input buffer circuitry on an integrated circuit that receives signals from an external source.

BACKGROUND OF THE INVENTION

High performance digital integrated circuits, including dynamic RAMs, have traditionally employed specialized circuits for receiving data from an external source. The digital signals produced by the external source are continuously changing and are considered to be valid only during certain intervals. Data receiving circuits (also known as input buffers) are used to capture the data from the external source during these periods of validity so that the integrated circuit may continue to utilize the captured data even though the external source is no longer providing a valid digital data signal.

The interface between an integrated circuit and the external circuitry is often controlled by timing signals produced by clocks. These timing signals (or latch signals) have a high level, a low level, and a latch edge. The latch edge is created when the latch signal transitions from a high level to a low level or from a low level to a high level. Sometimes the latch signals and their edges are known as "strobes." For example, in dynamic RAM circuitry, these signals are called Row Address Strobe ("RAS") and Column Address Strobe ("CAS").

Data input to the integrated circuit is considered to be valid and stable only during a brief interval of time near a latch edge. At other times (known as transitioning times), the data is transitioning between valid states. During these transitioning times, the data input to the integrated circuit is not valid and should not be utilized.

One way to increase performance of the interface between integrated circuits and external circuitry is to decrease the time required to capture or "latch" the data from the external source.

Latching input buffers can be constructed in metal oxide semiconductor (MOS) technologies using dynamic circuit design techniques, such as precharging and latching cross-coupled pairs of MOS transistors with positive feedback.

Traditional dynamic latching input buffer circuits suffer from a number of disadvantages, including one or more of the following: (1) requiring use of multiple latch signals; (2) dissipation of DC power; (3) excess capacitance on critical (positive feedback) nodes; and (4) charge "kick-back" into the latching circuit inputs.

Figure 1 illustrates one prior art dynamic latching input buffer. An external signal Input is compared to a reference voltage V_{REF}. If the signal Input has a voltage level which exceeds V_{REF}, then the signal Output is asserted, otherwise complementary signal $\overline{\text{Output}}$ is asserted.

Latch1 is a latching signal. When the latching signal transitions from a high level to a low level, the latch signal is referred to as a falling edge signal. When the latching signal transitions from a low level to a high level, the latch signal is referred to as a rising edge signal.

The prior art shown in Figure 1 requires multiple latch signals (Latch1 and Latch2). Latch1 and Latch2 are often collectively referred to as multi-phase latch signals because of their timing relationship to each other. Latch1 and Latch2 should operate in a precisely timed relationship for maximum performance.

The circuit shown in Figure 1 may suffer from charge "kick-back." After Latch2 has risen, the voltages on nodes 130 and 140 have been amplified to approximately the full power supply levels. For example, if Input > V_{REF}, then the voltage at node 130, V_{130}, is approximately VDD.

When Latch1 rises and Latch2 falls, transistor 110 couples node 130 to Input, and transistor 120 couples node 140 to V_{REF}. The charge on node 130 flows back to the input terminal 112. The charge on node 140 similarly flows back to the reference voltage terminal 122. This charge "kick-back" can inject high frequency noise onto the Input signal and the V_{REF} signal. Since a number of data receivers are typically coupled to receive V_{REF}, this may result in substantial high frequency noise injected back onto the V_{REF} signal. This can create a data-dependent disturbance on V_{REF} which can be a factor in causing the data receivers to malfunction on the next latch cycle.

Figure 2 illustrates another dynamic latching input buffer according to the prior art. As in Figure 1, the external signal Input is compared against a reference voltage V_{REF}.

One disadvantage of this prior art is that it dissipates DC power. The voltages captured on nodes 230 and 240 keep transistors 210 and

220 turned on while Latch1 is low. Therefore, either Output at node 250 or $\overline{\text{Output}}$ at node 260 is driven to VDD. Thus either transistor 210 or 220 may provide a current path from VDD to VSS, resulting in undesirable d.c. power dissipation.

A second disadvantage of this circuit is the capacitive loading on the critical cross-coupled nodes Output 250 and $\overline{\text{Output}}$ 260. In Figure 2, these nodes are connected to two MOSFET gates and four MOSFET drains (in addition to the next stage of logic circuitry which is not shown). This capacitance may slow down circuit operation.

SUMMARY AND OBJECTS OF THE INVENTION

One of the objectives of the present invention is to provide latching input buffer circuitry that requires only a single latch signal.

Another object of the invention is to provide latching input buffer circuitry that dissipates substantially zero DC power.

Another object of the invention is to provide latching input buffer circuitry that minimizes capacitance loading on critical (positive feedback) nodes of the input buffer circuitry.

Another object of the invention is to provide latching input buffer circuitry that minimizes charge "kick-back" into the input buffer circuitry inputs.

Another object of the invention is to provide latching input buffer circuitry that minimizes capacitive "kick-back" into the input buffer circuitry inputs.

A metal-oxide semiconductor dynamic latching input buffer is described. The input buffer latches a data signal in response to a single latch signal. A precharging circuit precharges an output terminal. An input sampler provides a sampled data voltage from the data signal in response to an edge of the latch signal. The sampled data voltage is substantially independent of the data signal after the latch signal is received. A reference voltage sampler provides a sampled reference voltage from a reference voltage in response to the latch edge. The sampled reference voltage is substantially independent of the data signal after the latch signal is received. A comparator provides an output signal indicating the greater of the sampled reference voltage

and the sampled data voltage. The comparator and the input and reference voltage samplers cooperate such that the input buffer d.c. power consumption is substantially zero.

Other objects, features and advantages of the present invention will be apparent from the accompanying drawings and from the detailed description which follows below.

BRIEF DESCRIPTION OF THE DRAWINGS

The present invention is illustrated by way of example and not limitation in the figures of the accompanying drawings, in which like references indicate similar elements and in which:

Figure 1 is a schematic of a prior art dynamic latching input buffer.

Figure 2 is a schematic of a prior art improvement of the circuitry of Figure 1.

Figure 3 illustrates one embodiment of the dynamic latching input buffer.

Figure 4 illustrates an alternative embodiment of the dynamic latching input buffer.

Figure 5 illustrates an alternative embodiment of the dynamic latching input buffer.

Figure 6 illustrates an alternative embodiment of the dynamic latching input buffer.

DETAILED DESCRIPTION

One embodiment of the present invention is illustrated in Figure 3. When the Latch signal is low, the Output 560 and $\overline{\text{Output}}$ 565 nodes are precharged to VDD by PMOS transistors 570 and 585. This balances and equalizes the circuit in preparation for the rising edge of the Latch signal. During precharge, when Latch is low, NMOS transistors 520 and 530 are off, thus ensuring that no DC current path exists while precharging.

When the Latch signal rises, transistors 520 and 530 turn on. Current begins to flow through transistors 540, 520, and 500 as well as through 550, 530, and 510. These currents cause the voltage levels of the Output 560 and $\overline{\text{Output}}$ 565 nodes to be substantially less than VDD.

In other words, the Latch signal is applied to gates 522, 532 of transistors 520 and 530, respectively. When the Latch signal has a high level, transistors 520 and 530 are turned on. When transistor 520 is turned on, current can flow from the drain 524 to the source 526. Likewise with transistor 530.

If the Input voltage is greater than the V_{REF} voltage, transistor 500 will be turned on "harder" than transistor 510 (i.e., the drain-to-source resistance of 500 will be less than the drain-to-source resistance of 510). Thus more current will flow through 540, 520, and 500 than through 550, 530, and 510. This causes the voltage at the $\overline{\text{Output}}$ node 565 to decrease faster than the voltage at the Output node 560. Thus a

voltage difference is established between the Output 560 and $\overline{\text{Output}}$ 565 nodes.

Cross-coupled transistors 575 and 580 amplify this voltage difference. Cross-coupled transistors 540 and 550 also amplify this voltage difference.

Transistors 575 and 580 are connected in a positive feedback configuration. As voltage at the $\overline{\text{Output}}$ node 565 decreases, the gate-to-source voltage on transistor 580, V_{GS-580}, increases. This in turn causes the voltage at the Output node 560 to rise. When the Output voltage rises, the gate-to-source voltage on transistor 575, V_{GS-575}, decreases. The decreasing voltage V_{GS-575} causes the voltage on the $\overline{\text{Output}}$ node 565 to decrease even further.

Transistors 540 and 550 are also cross-coupled in a positive feedback configuration. This increases the gain and the gain-bandwidth product of the circuit, thus helping to increase the speed and the sensitivity of the latching input buffer circuitry.

Transistors 500 and 510 should operate in the "triode region" (nonsaturation region). The voltage drop across 500 should be smaller than the voltage drop across 540. Thus the drain-to-source voltage of 500, V_{DS-500}, should be smaller than the drain-to-source voltage of 540, V_{DS-540}. Similarly, the voltage drop across 510 should be smaller than the drop across 550. (In other words, $V_{DS-510} < V_{DS-550}$). This allows cross-coupled amplifier transistors 540 and 550 to have increased gain and bandwidth. This in turn helps to increase the speed and the

sensitivity of the latching input buffer circuitry. The lower voltage drop across 500 and 510 also minimizes charge kick-back.

The voltage difference between the Output node 560 and $\overline{\text{Output}}$ node 565 is amplified until the Output and $\overline{\text{Output}}$ signal voltages approximate power supply limits. Assume the voltage level at the Output node 560 is approximately VDD and that the voltage level at the $\overline{\text{Output}}$ node 565 is approximately VSS. In this case transistors 550 and 575 will be turned off and transistors 540 and 580 will be on. In particular, transistor 550 is turned off while 540 is on. There is no DC current path from VDD to VSS. Thus the Output node cannot be forced from a high level to a low level because transistor 550 is cut off.

If instead, the voltage level at the $\overline{\text{Output}}$ node 565 is approximately VDD and the voltage level at the Output node 560 is approximately VSS, there is still no DC current path. In this case 540 will be turned off and the $\overline{\text{Output}}$ node 565 cannot be forced to a low level.

The capacitive loading on the cross-coupled output nodes, Output 560 and $\overline{\text{Output}}$ 565 is also important for speed concerns. In Figure 3, note that the $\overline{\text{Output}}$ node is connected to two MOSFET gates (552 and 582), three MOSFET drains (544, 578, 573) and the next logic stage (not shown). The count is identical for the Output node 560. The Output node 560 is connected to two MOSFET gates (542 and 577), three MOSFET drains (554, 583, 588) and the next logic stage (not shown).

As illustrated in Figure 3, the present embodiment uses only a single latch signal, Latch. As discussed previously, this is advantageous when the highest performance is desired because it eliminates problems with phase-to-phase skew, especially in the presence of long latch signal lines having non-negligible metallization RC delay and waveshape distortion.

As mentioned above, the present embodiment has minimal charge kick-back into the input nodes 502 and 512. In Figure 1, Input and V_{REF} were connected to nodes that were previously charged to VDD or VSS thus forcing charge to be kicked back into Input and V_{REF}. No such connection is illustrated in Figure 3.

The present embodiment also has minimal capacitive kick-back into the inputs. The input signals, Input and V_{REF}, are coupled to the gates of grounded-source transistors, so the primary mechanism for capacitive kick-back is gate-to-drain capacitive coupling. In the present embodiment, the transistor sizes are selected so that the voltage at the drains 526, 514 of the input transistors 500 and 510, respectively, does not fluctuate significantly and therefore the drain-to-gate charge injection is small.

An alternative embodiment is illustrated in Figure 4. For Figure 4, the NMOS and PMOS transistors of Figure 3 have been replaced with their complements (PMOS and NMOS, respectively).

In Figure 3, the latching circuit is activated by a rising edge of the Latch signal. In Figure 4, the latching circuit is activated by a falling edge of the Latch signal.

The NMOS transistors 520, 530, 540, and 550 of Figure 3 tend to be faster than the PMOS transistors 620, 630, 640, and 650 of Figure 4 due to carrier mobility in NMOS transistors being higher than carrier mobility in PMOS transistors. Use of NMOS transistors helps to ensure faster latching operation.

Referring to Figure 3, the common-mode voltage of the input signals, Input and V_{REF}, should be near VDD (or VSS when using the circuitry of Figure 4). This helps to ensure that transistors 500 and 510 receive a gate-to-source voltage which will place each of them in the triode region of operation. One way of achieving such a common-mode input voltage is to use the circuitry in an application where the interface levels are defined to be at or near the power supply voltages. Some examples include current mode logic (CML), Gunning transceiver logic (GTL), Rambus signaling levels (RSL), and so forth.

Another way of helping to ensure that the circuitry of Figure 3 receives a large common-mode input voltage is to precede the circuitry by a preamplifier which has a large (near power supply levels) common-mode output voltage.

Some CMOS fabrication processes contain an optional step which can be advantageously exploited in the present embodiment. In addition to the normal NMOS transistor with the typical threshold voltage ($V_{TH} \approx +0.6$ volts), these processes offer a second NMOS transistor (variously called "natural," "unimplanted," or "zero threshold") with a low threshold voltage ($-0.15 < V_{TH} < +0.15$ volts). Using such low threshold voltage transistors for transistors 500 and 510 in Figure 3

will help to improve operation at lower values of common-mode input voltage.

Even if transistors 500 and 510 have a threshold voltage less than zero volts, there will still not be any substantial DC power dissipation. This is because transistors 540 and 550 cut off the DC current path. As long as 540 and 550 are enhancement mode transistors (i.e. having a threshold voltage above zero), the DC power dissipation will be approximately zero.

Referring to Figure 3, other alternative embodiments involve rearranging the sequence of the series-coupled transistors, 500, 520, and 540 and their respective counterparts 510, 530, and 550.

One such embodiment is shown in Figure 5 where transistors 500 and 520 have switched positions from their respective locations in Figure 3. Likewise, transistors 510 and 530 have also exchanged positions from their respective locations in Figure 3.

Another such embodiment is shown in Figure 6 where the series order of transistors 500, 520, and 540 in Figure 3 has been altered so that transistor 540 is serially coupled between transistors 520 and 500. Similarly, transistor 550 has been repositioned between transistors 530 and 510.

In the foregoing specification, the invention has been described with reference to specific exemplary embodiments thereof. It will, however, be evident that various modifications and changes may be made thereto without departing from the broader spirit and scope of the invention as set forth in the claims. The specification and drawings are,

accordingly, to be regarded in an illustrative rather than a restrictive sense.

CLAIMS

What is claimed is:

1. In a metal-oxide semiconductor integrated circuit, a dynamic latching input buffer for latching a data signal in response to a single latch signal, comprising:

a precharging circuit for precharging an output terminal, the precharging circuit coupled to a power supply, the power supply having a first terminal and a second terminal;

an input sampler providing a sampled data voltage from the data signal in response to an edge of the latch signal, wherein the sampled data voltage is substantially independent of the data signal after the latch signal is received;

a reference voltage sampler providing a sampled reference voltage from a reference voltage in response to the edge of the latch signal, wherein the sampled reference voltage is substantially independent of the reference voltage signal after the latch signal is received;

a comparator providing an output signal indicating the greater of the sampled reference voltage and the sampled data voltage, wherein the comparator and the input and reference voltage samplers cooperate such that an input buffer d.c. power consumption is substantially zero.

2. The dynamic latching input buffer of claim 1, wherein:

(a) the latch signal having a first level, a second level and a latch edge;

(b) the precharging circuit controls the input buffer d.c. power consumption to be substantially zero when the latch signal is at a first level;

(c) the comparator controls the input buffer d.c. power consumption to be substantially zero when the latch signal is at a second level.

3. The dynamic latching input buffer of claim 2, wherein the precharging circuit further comprises:

a first transistor, wherein a first terminal of the first transistor is coupled to the first terminal of the power supply, a gate of the first transistor is coupled to receive the latch signal, a second terminal of the first transistor is coupled to the comparator; and

a second transistor, wherein a first terminal of the second transistor is coupled to the first terminal of the power supply, a gate of the second transistor is coupled to receive the latch signal, a second terminal of the second transistor is coupled to the comparator, wherein the second terminal of the second transistor forms the output terminal.

4. The dynamic latching input buffer of claim 3 wherein the first and second transistors are PMOS transistors.

5. The dynamic latching input buffer of claim 3 wherein the first and second transistors are NMOS transistors.

6. The dynamic latching input buffer of claim 2, wherein the input sampler comprises:

a first transistor, wherein a first terminal of the first transistor is coupled to the comparator, a gate of the first transistor is coupled to receive the latch signal;

a second transistor, wherein a first terminal of the second transistor is coupled to a second terminal of the first transistor, a gate of the second transistor is coupled to receive the data input signal, and a second terminal of the second transistor is coupled to the second terminal of the power supply.

7. The dynamic latching input buffer of claim 2, wherein the reference voltage sampler comprises:

a first transistor, wherein a first terminal of the first transistor is coupled to the comparator, a gate of the first transistor is coupled to receive the latch signal;

a second transistor, wherein a first terminal of the second transistor is coupled to a second terminal of the first transistor, a gate of the second transistor is coupled to receive the reference voltage signal, and a second terminal of the second transistor is coupled to the second terminal of the power supply.

8. The dynamic latching input buffer of claims 6 or 7 wherein the first and second transistors are PMOS transistors.

9. The dynamic latching input buffer of claims 6 or 7 wherein the first and second transistors are NMOS transistors.

10. The dynamic latching input buffer of claim 9 wherein the second transistor is a low threshold voltage NMOS transistor having a threshold voltage between -0.15 volts and +0.15 volts.

11. The dynamic latching input buffer of claim 2, wherein the comparator comprises:

a first transistor, wherein a first terminal of the first transistor is coupled to the first terminal of the power supply;

a second transistor, wherein a first terminal of the second transistor is coupled to the first terminal of the power supply, a second terminal of the second transistor is coupled to a gate of the first transistor, a second terminal of the first transistor is coupled to a gate of the second transistor;

a third transistor, wherein a first terminal of the third transistor is coupled to the second terminal of the first transistor, a second terminal of the third transistor is coupled to the input sampler; and

a fourth transistor, wherein a first terminal of the fourth transistor is coupled to the second terminal of the second transistor and a gate of the third transistor, a gate of the fourth transistor is coupled to the first terminal of the third transistor, a second terminal of the fourth transistor is coupled to the reference voltage sampler.

12. The dynamic latching input buffer of claim 11, wherein the first and second transistors are a first type of transistor and the third and fourth transistors are a second type of transistor.

13. The dynamic latching input buffer of claim 11, wherein the first type of transistor is an NMOS transistor and the second type of transistor is a PMOS transistor.

14. The dynamic latching input buffer of claim 11, wherein the first type of transistor is a PMOS transistor and the second type of transistor is an NMOS transistor.

15. The dynamic latching input buffer of claim 11 wherein the input sampler comprises:

a fifth transistor, wherein a first terminal of the fifth transistor is coupled to the second terminal of the third transistor, a gate of the fifth transistor is coupled to receive the latch signal;

a sixth transistor, wherein a first terminal of the sixth transistor is coupled to a second terminal of the fifth transistor, a gate of the sixth transistor is coupled to receive the data input signal, and a second terminal of the sixth transistor is coupled to the second terminal of the power supply, wherein the fifth transistor is selected to have a magnitude of a first-to-second terminal voltage less than a magnitude of a first-to-second terminal voltage of the third transistor.

16. The dynamic latching input buffer of claim 11 wherein the reference voltage sampler comprises:

a fifth transistor, wherein a first terminal of the fifth transistor is coupled to the second terminal of the fourth transistor, a gate of the fifth transistor is coupled to receive the latch signal;

a sixth transistor, wherein a first terminal of the sixth transistor is coupled to a second terminal of the fifth transistor, a gate of the sixth transistor is coupled to receive the reference voltage, and a second terminal of the sixth transistor is coupled to the second terminal of the power supply, wherein the fifth transistor is selected to have a

magnitude of a first-to-second terminal voltage less than a magnitude of a first-to-second terminal voltage of the third transistor.

17. The dynamic latching input buffer of claims 15 or 16 wherein:

(a) the first and second transistors are a first type of transistor;

(b) the third, fourth, fifth and sixth transistors are a second type of transistor.

18. The dynamic latching input buffer of claim 17 wherein the first type of transistor is a PMOS transistor and the second type of transistor is an NMOS transistor.

19. The dynamic latching input buffer of claim 17 wherein the first type of transistor is an NMOS transistor and the second type of transistor is a PMOS transistor.

20. The dynamic latching input buffer of claim 2 including a complementary output terminal wherein:

the complementary output terminal is coupled to the precharging circuitry, the complementary output terminal providing a complementary output signal which is a logical complement of the output signal.

21. A dynamic latching input buffer for latching a data signal in response to a single latch signal, comprising:

a precharging circuit for precharging an output terminal;

an input sampler providing a sampled data voltage from the data signal in response to an edge of the latch signal;

a reference voltage sampler providing a sampled reference voltage from a reference voltage in response to the edge of the latch signal;

a comparator providing an output signal indicating the greater of the sampled reference voltage and the sampled data voltage, wherein the comparator and the input and reference voltage samplers cooperate such that an input buffer d.c. power consumption is substantially zero.

22. The dynamic latching input buffer of claim 21 wherein the input and reference voltage samplers are each serially coupled between the comparator and a power supply.

23. The dynamic latching input buffer of claim 21 wherein the precharging circuit is coupled to a first terminal of a power supply, wherein the input and reference voltage samplers are each serially coupled between the precharging circuit and a second terminal of the power supply.

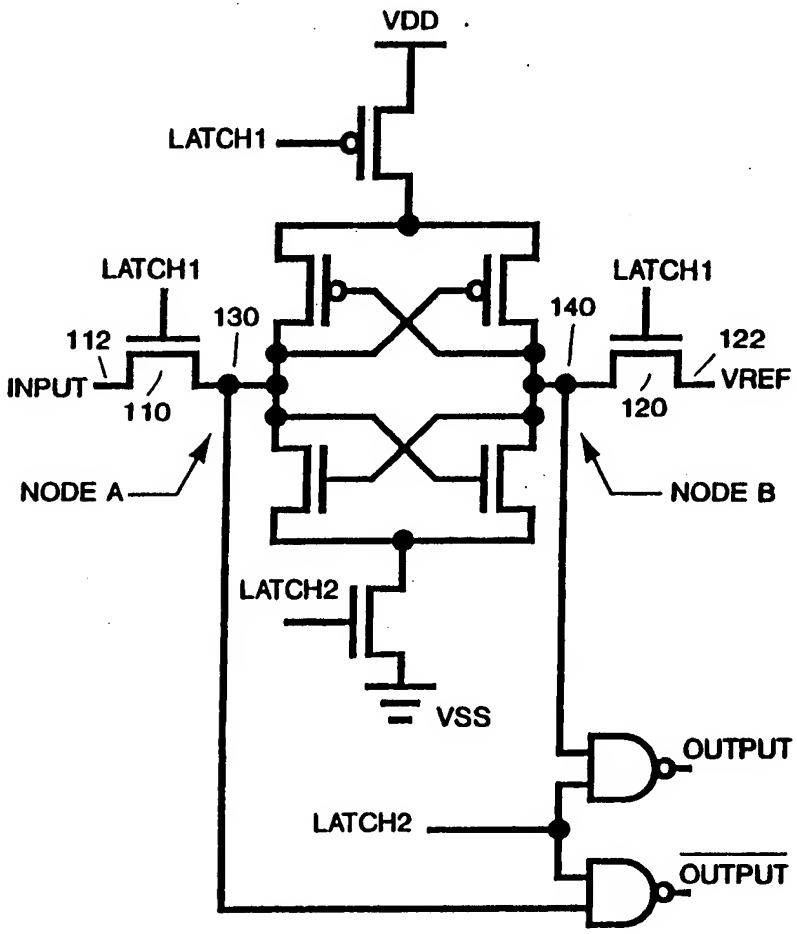


FIG. 1
PRIOR ART

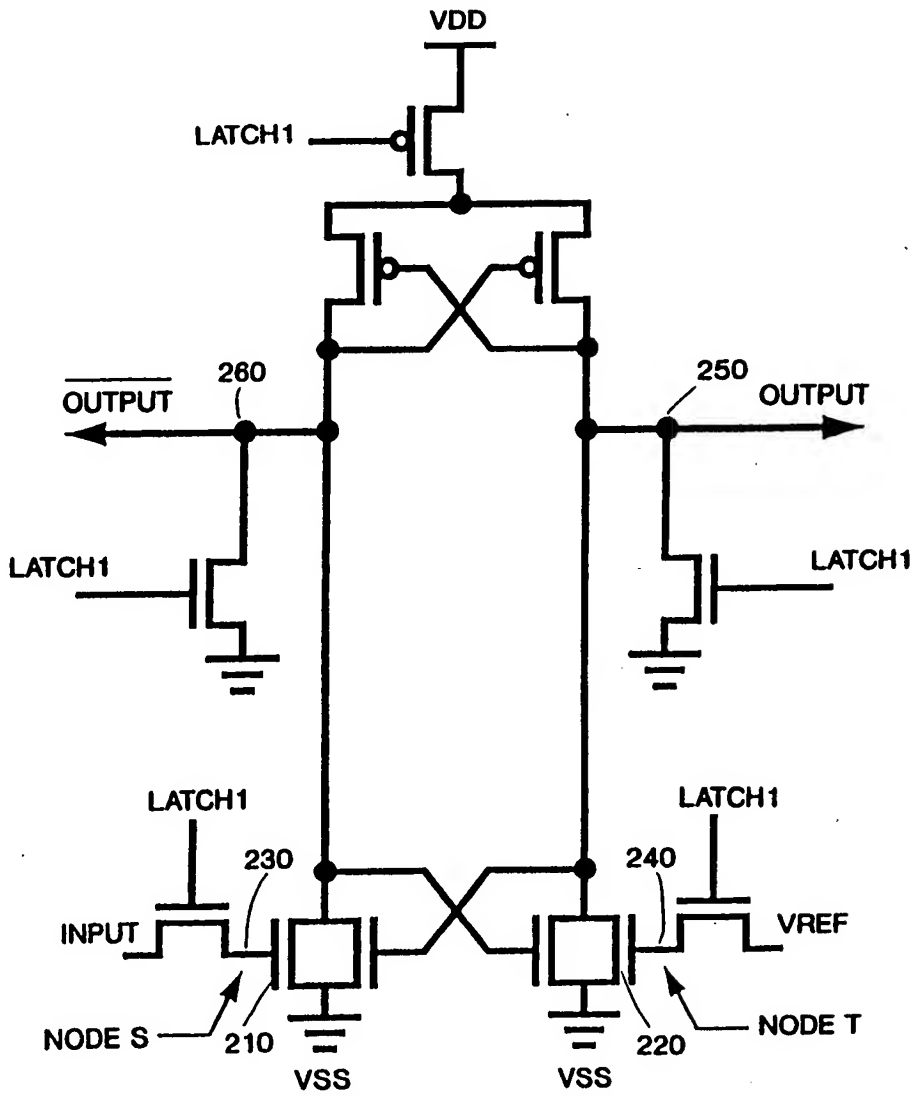


FIG. 2
PRIOR ART

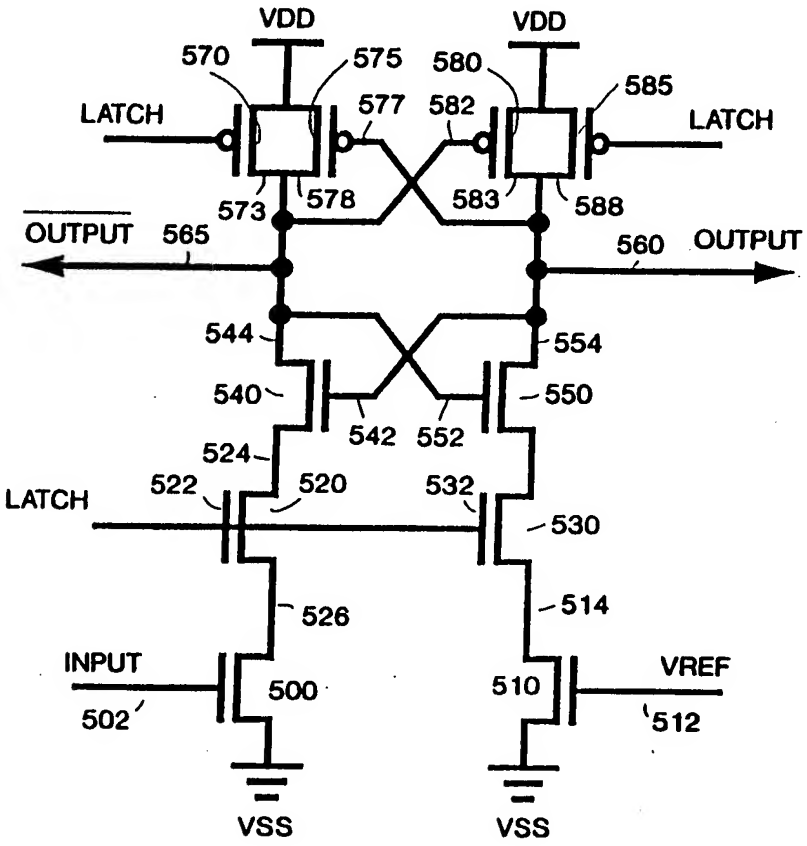

VDD
VDD
570
575
580
585
LATCH
577
582
LATCH
573
578
583
588
OUTPUT
565
560
OUTPUT
544
554
540
550
542
552
524
LATCH
522
520
532
530
526
514
INPUT
500
510
VREF
502
512
VSS
VSS

FIG. 3

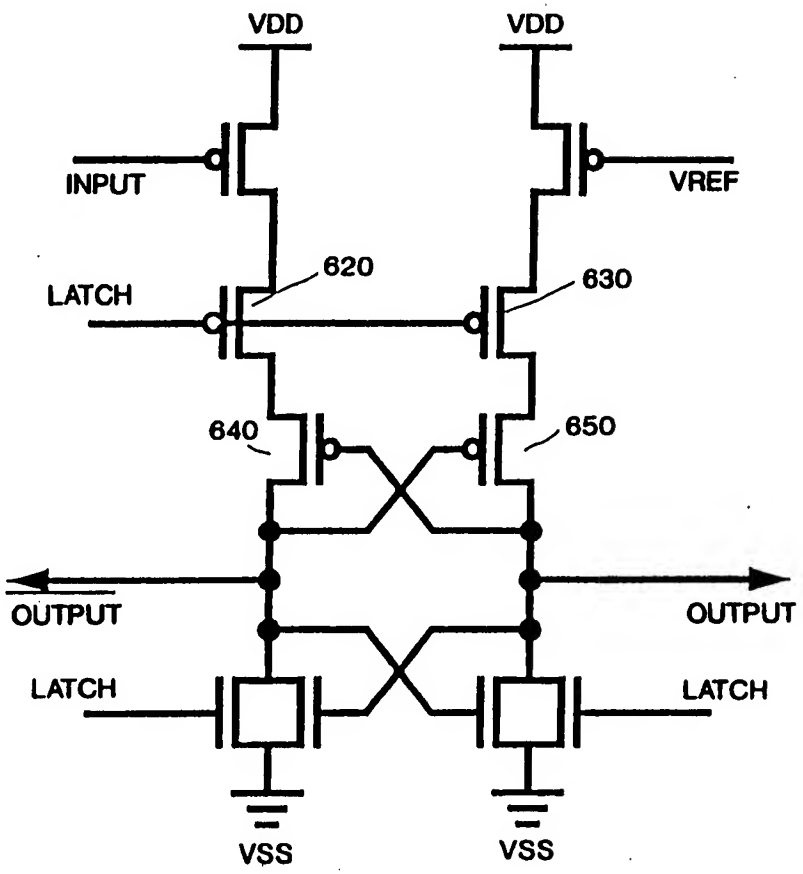

VDD
VDD
INPUT
VREF
LATCH
620
630
640
650
OUTPUT
OUTPUT
LATCH
LATCH
VSS
VSS

FIG. 4

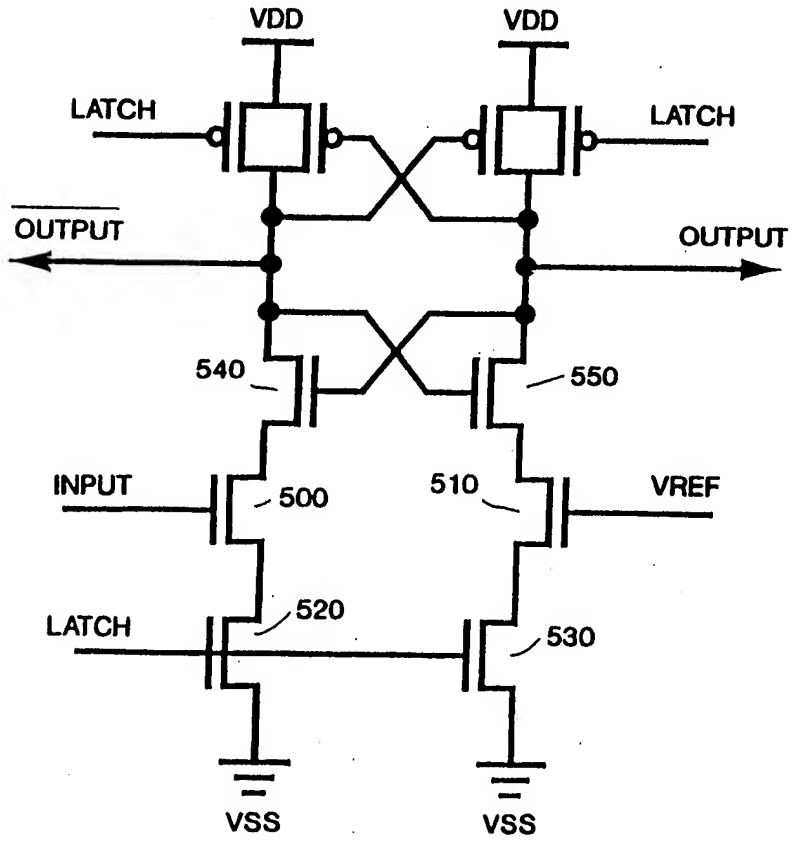

VDD
VDD
LATCH
LATCH
OUTPUT
OUTPUT
540
550
INPUT
500
510
VREF
LATCH
520
530
VSS
VSS

FIG. 5

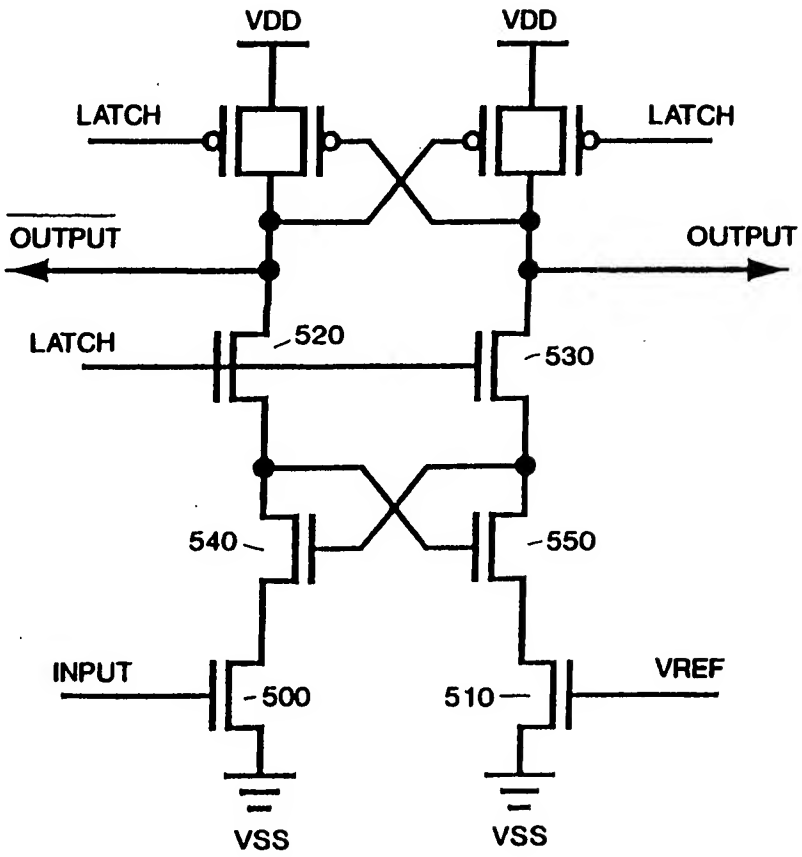

VDD
VDD
LATCH
LATCH
OUTPUT
OUTPUT
LATCH
520
530
540
550
INPUT
500
510
VREF
VSS
VSS

FIG. 6

INTERNATIONAL SEARCH REPORT | PCT/US 95/12094

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H03K3/356

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H03K

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
X	US,A,4 973 864 (NOGAMI) 27 November 1990 see column 4, line 27 - column 6, line 18 see column 9, line 3 - column 10, line 28 see figures 3,11-14	1-9, 11-23
Y	---	10
Y	US,A,5 132 567 (PURI ET AL.) 21 July 1992 see column 2, line 53 - line 68; figure 3	10
X	---	
	EP,A,0 407 591 (OKI ELECTRIC INDUSTRY CO., LTD.) 16 January 1991 see page 5, line 8 - page 8, line 21; figure 1	1-4,6,7, 9,11,12, 14-18, 20-23

☐ Further documents are listed in the continuation of box C. ☒ Patent family members are listed in annex.

* Special categories of cited documents :

"A" document defining the general state of the art which is not considered to be of particular relevance

"E" earlier document but published on or after the international filing date

"L" document which may throw doubts on priority claim(s) or which is cited to establish the publication date of another citation or other special reason (as specified)

"O" document referring to an oral disclosure, use, exhibition or other means

"P" document published prior to the international filing date but later than the priority date claimed

"T" later document published after the international filing date or priority date and not in conflict with the application but cited to understand the principle or theory underlying the invention

"X" document of particular relevance; the claimed invention cannot be considered novel or cannot be considered to involve an inventive step when the document is taken alone

"Y" document of particular relevance; the claimed invention cannot be considered to involve an inventive step when the document is combined with one or more other such documents, such combination being obvious to a person skilled in the art.

"&" document member of the same patent family

Date of the actual completion of the international search	Date of mailing of the international search report
19 January 1996	08.02.96

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+ 31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+ 31-70) 340-3016	Cantarelli, R

Form PCT/ISA/210 (second sheet) (July 1992)

Patent document cited in search report	Publication date	Patent family member(s)		Publication date
US-A-4973864	27-11-90	JP-A-	2024898	26-01-90
		JP-B-	7027717	29-03-95
US-A-5132567	21-07-92	EP-A-	0509283	21-10-92
		JP-A-	4346515	02-12-92
EP-A-407591	16-01-91	WO-A-	9004286	19-04-90
		US-A-	5192878	09-03-93